Introduction to VHDL

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1. VHDL : VHSIC HDL

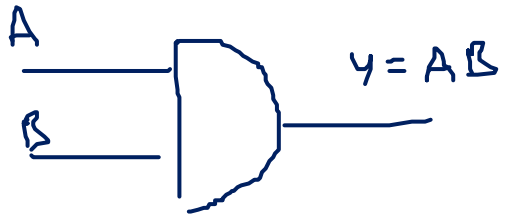
↳ Very High Speed Integrated Circuit Hardware Description Language.

→ consists of entity, architecture.

2. Verilog HDL :- Consists of modules

VHDL :- HDL

AND



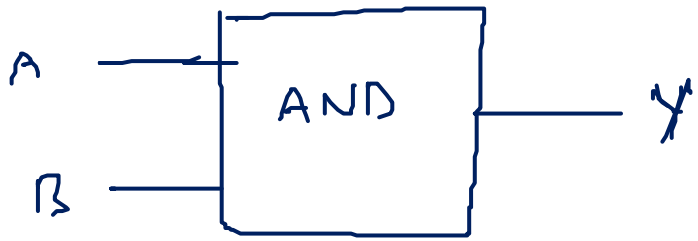
Y <= A AND B;

↓

Operator.

* It consists of two parts —— 1. entity
2. Architecture

Entity declaration :-



→ entity describes the inputs and output ports of a logic module & provides external view of component.

Syntax:

```
entity entityname is
    [generic_declaration]
    [port_clause]
    [entity declarative items]
end entityname;
```

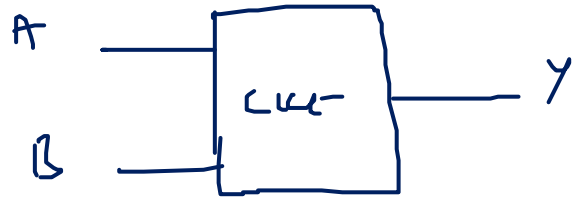
where the "generic_declaration" declares constants that can be used to control the structure or behaviour of the entity.

Syntax for generic :-

generic (constant_name : subtype_indication [:= value]
{; const_name : subtype_indication [:= value]}
);

The port_clause specifies the interface channels of the entity.

Syntax :- port (port-name : [mode] subtype_indication ;
:
);



port (A : IN std_logic ;
B : in " ;
Y : out ");

The entity_declarative_items declares some constants, types or signals that can be used in the implementation of the entity

Example:-

```
entity full_adder is
    port( A, B, Cin : in Bit;
          S, Cout : out Bit);
end full_adder;
```